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Express Mail No. EV 534 877 643 US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of: Perino et al.

Confirmation No.: 4507

Application No.: 09/961,114

Group Art No.: 2833

Filed: September 20, 2001

Examiner: Figueroa, Felix O.

For: *Chip Socket and Chip File Assembly
for Semiconductor Chips*

Attorney Docket No.: **60809-5054-US**
(formerly RB1-035USC3US)

TRANSMITTAL OF REVOCATION AND POWER OF ATTORNEY

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant's representative encloses herewith a Revocation and Power of Attorney for the application number listed above. Applicant's attorney requests that the Power of Attorney be accepted and made of record.

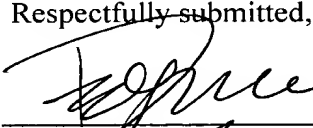
Future correspondence should be forwarded to:

Customer No. 38426

No fee is believed owed with this submission. The Commissioner is authorized to charge any fees associated with this communication to our deposit account number 50-0310 (order no. 60809-5054-US). A copy of this sheet is enclosed for such purpose.

Respectfully submitted,

Date July 7, 2005



Dion M. Bregman
MORGAN, LEWIS & BOCKIUS LLP
2 Palo Alto Square
3000 El Camino Real, Suite 700
Palo Alto, California 94306
(640) 843-4000

Reg. No. 45,645

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE



Application of: See Schedule A

Serial No.: See Schedule A

Filed: See Schedule A

For: See Schedule A

Attorney Docket No: See Schedule A

REVOCATION AND POWER OF ATTORNEY

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

S I R:

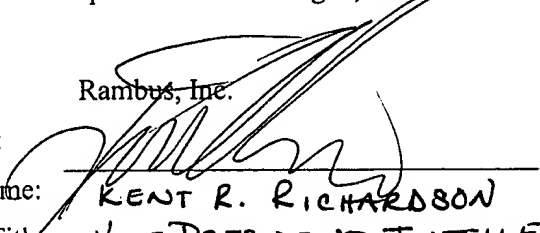
Rambus, Inc. owner of the entire right, title and interest in, to and under the inventions listed in Schedule A hereby revokes all previous powers of attorney and appoints Morgan, Lewis & Bockius LLP, **Customer No. 38426**, and each of them, its attorneys, prosecute these matters, and to transact all business in the Patent and Trademark Office connected therewith, said appointment to be to the exclusion of the inventors and their attorney(s) in accordance with the provisions of 37 C.F.R. 3.71, provided that, if any one of these attorneys ceases being affiliated with the law firm of Morgan, Lewis & Bockius LLP as partner, counsel, or employee, then the appointment of that attorney and all powers derived therefrom shall terminate on the date such attorney ceases being so affiliated.

In addition, the undersigned assignee also appoints Kent R. Richardson (Reg. No. 39,443), Paul M. Anderson (Reg. No. 39,896), Paula J. Lagattuta (Reg. No. 40,691), Jose G. Moniz (Reg. 50,192) and Lance Kreisman (Reg. No. 39,256) of Rambus Inc., to prosecute these matters and to transact all business in the Patent and Trademark Office connected therewith.

Please direct all future correspondence to the address associated with Customer No. 38426, Morgan, Lewis & Bockius LLP and direct all telephone calls to Morgan, Lewis & Bockius LLP at (650) 843-4000.

Date: 6/30/05

Assignee: Rambus, Inc.

Signature: 

Typed Name: KENT R. RICHARDSON

Position/Title: VICE PRESIDENT INTELLECTUAL

Address: 4440 El Camino Real
Mountain View, California 94022

PROPERTY

SCHEDULE A

Serial No./ Patent No.	Filing Date/ Issue Date	Title	First Named Inventor	Attorney Docket No.
09/468,247 6,352,435	12/20/1999 03/05/2002	Chip Socket Assembly and Chip File Assembly for Semiconductor Chips (RA041.C1D1.US)	Donald V. Perino	60809-5051-US
09/957,815 6,619,973	09/20/2001 09/16/2003	Chip Socket Assembly and Chip File Assembly for Semiconductor Chips (RA041.C1D1C1.US)	Donald V. Perino	60809-5052-US
09/957,822 6,589,059	09/20/2001 07/08/2003	Chip Socket Assembly and Chip File Assembly for Semiconductor Chips (RA041.C1D1C2.US)	Donald V. Perino	60809-5053-US
09/961,114	09/20/2001	Chip Socket Assembly and Chip File Assembly for Semiconductor Chips (RA041.C1D1C3.US)	Donald V. Perino	60809-5054-US
09/594,221	06/14/2000	Method and Apparatus for Transmitting Data with Reduced Coupling Noise (RA163.P.US)	Mark A. Horowitz	60809-5055-US
11/130,502	05/17/2005	Method and Apparatus for Transmitting Data with Reduced Coupling Noise (RA163.CA.US)	Mark A. Horowitz	60809-5056-US
09/817,828 6,590,781	03/26/200 07/08/2003	Clock Routing in Multiple Channel Modules and Bus Systems (RA171.CIP1.US)	Ravindranath T. Kollipara	60809-5057-US
10/420,308	04/22/2003	Clock Routing in Multiple Channel Modules and Bus Systems (RA171.CIP1D1.US)	Ravindranath T. Kollipara	60809-5058-US
09/679,143 6,674,161	10/03/2000 01/06/2004	Semiconductor Stacked Die Devices (RA189.P.US)	Belgacem Haba	60809-5060-US
10/706,897 6,902,953	11/13/2003 06/07/2005	Methods of Forming Semiconductor Stacked Die Devices (RA189.D1.US)	Belgacem Haba	60809-5061-US
11/123,641	05/06/2005	Semiconductor Stacked Die Devices and Methods for Forming Semiconductor Stacked Die Devices (RA189.D1C1.US)	Belgacem Haba	60809-5062-US
10/438,238	05/14/2003	Multilayer Flip-Chip Substrate Interconnect Layout (RA291.P.US)	Hao Shi	60809-5063-US